HSP50110/210EVAL Output Formatter Control Signal

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Introduction

This document more explicitly defines the output interface of the HSP50110/210EVAL board, as set by the Output Multiplexer Control Register. The AOUT and BOUT Output Busses are defined at the bit level and the signals that are mapped to these bits are defined. Pinouts are given for both the P2 and JP5 connectors. Applications for the various signals are provided. This data was collected from both the HSP50210 Data Sheet and the HSP50110/210EVAL User's Manual. The HSP50110/210EVAL User's Manual has the following entry for the Output Control Register:

Item 26: Output Multiplexer Control

The output multiplexer selects the signals that are routed to the output bus of the HSP50210. In most cases, the soft decisions are available at the MSB's of the AOUT bus. This allows other nodes to be monitored without disturbing the output data. In most cases where an error detector is brought out, it is the bottom 7 bits of the BOUT bus. Selection 7 can be used to plot the I/Q constellation using a logic analyzer or a pair of D/A converters.

0 - ISOFT(2:0), QSOFT(2:0), STATUS(6:0), AGC(7:1)

1 - ISOFT2, QSOFT2, MAG(7:0), STATUS6, STATUS0, PHASE(7:0)

2 - ISOFT(2:0), QSOFT(2:0), STATUS(6:0), FREQERR(7:1)

3 - ISOFT(2:0), QSOFT(2:0), STATUS(6:0), GAINERR(7:1)

4 - ISOFT(2:0), QSOFT(2:0), STATUS(6:0), BITPHERR(7:1)

5 - ISOFT(2:0), QSOFT(2:0), STATUS(6:0), CARPHERR(7:1)

6 - ISOFT(2:0), QSOFT(2:0), LKACC(6:0), LKCNT(6:0)

7 - ISOFT(2:0), QSOFT(2:0), IEND(7:1), QEND(7:1)

8 - RESERVED(7:0), STATUS5, STATUS6, NCOCOS9-0

NOTE: Table 1 defines the AOUT bus, while Table 2 defines the BOUT bus.

TABLE 1. AOUT BIT DEFINITIONS

OUTPUT SELECT	AOUT 9	AOUT 8	AOUT 7	AOUT 6	AOUT 5	AOUT 4	AOUT 3	AOUT 2	AOUT 1	AOUT 0
P2 Pins	C19	A19	C18	A18	C17	A17	C16	A16	A15	C14
JP5 Pins	5	6	7	8	9	10	11	12	13	14
0000	ISOFT2	ISOFT1	ISOFT0	QSOFT2	QSOFT1	QSOFT0	STATUS6	STATUS5	STATUS4	STATUS3
0001	ISOFT2	QSOFT2	MAG7	MAG6	MAG5	MAG4	MAG3	MAG2	MAG1	MAG0
0010	ISOFT2	ISOFT1	ISOFT0	QSOFT2	QSOFT1	QSOFT0	STATUS6	STATUS5	STATUS4	STATUS3
0011	ISOFT2	ISOFT1	ISOFT0	QSOFT2	QSOFT1	QSOFT0	STATUS6	STATUS5	STATUS4	STATUS3
0100	ISOFT2	ISOFT1	ISOFT0	QSOFT2	QSOFT1	QSOFT0	STATUS6	STATUS5	STATUS4	STATUS3
0101	ISOFT2	ISOFT1	ISOFT0	QSOFT2	QSOFT1	QSOFT0	STATUS6	STATUS5	STATUS4	STATUS3
0110	ISOFT2	ISOFT1	ISOFT0	QSOFT2	QSOFT1	QSOFT0	LKACC6	LKACC5	LKACC4	LKACC3
0111	ISOFT2	ISOFT1	ISOFT0	QSOFT2	QSOFT1	QSOFT0	Iend7	Iend6	Iend5	Iend4
1000	RSRVD7	RSRVD6	RSRVD5	RSRVD4	RSRVD3	RSRVD2	RSRVD1	RSRVD0	STATUS5	STATUS6

TABLE 2. BOUT BIT DEFINITIONS

OUTPUT SELECT	BOUT 9	BOUT 8	BOUT 7	BOUT 6	BOUT 5	BOUT 4	BOUT 3	BOUT 2	BOUT 1	BOUT 0
P2 Pins	A10	C9	A9	C8	A8	C7	A7	C6	C5	A5
JP5 Pins	17	18	19	20	21	22	23	24	25	26
0000	STATUS2	STATUS1	STATUS0	AGC7	AGC6	AGC5	AGC4	ACG3	AGC2	AGC1
0001	STATUS6	STATUS0	PHASE7	PHASE6	PHASE5	PHASE4	PHASE3	PHASE2	PHASE1	PHASE0
0010	STATUS2	STATUS1	STATUS0	FE7	FE6	FE5	FE4	FE3	FE2	FE1
0011	STATUS2	STATUS1	STATUS0	GE7	GE6	GE5	GE4	GE3	GE2	GE1
0100	STATUS2	STATUS1	STATUS0	TE7	TE6	TE5	TE4	TE3	TE2	TE1
0101	STATUS2	STATUS1	STATUS0	CARPE7	CARPE6	CARPE5	CARPE4	CARPE3	CARPE2	CARPE1
0110	LKACC2	LKACC1	LKACC0	LKCNT6	LKCNT5S	LKCNT4	LKCNT3	LKCNT2	LKCNT1	LKCNT0
0111	Iend3	Iend2	Iend1	Qend7	Qend6	Qend5	Qend4	Qend3	Qend2	Qend1
1000	NCOCOS9	NCOCOS8	NCOCOS7	NCOCOS6	NCOCOS5	NCOCOS4	NCOCOS3	NCOCOS2	NCOCOS1	NCOCOS0

NOTE: The output symbol clock used with the AOUT and BOUT busses are found on P2-C20 and JP5-29, with the associated ground found on P2-A20 and JP5-30.

Definition of Signal Bus Names

Data Signal Busses:

ISOFT(2:0) This bus is the I channel soft decision slicer output data, expressed in 2's complement format with one sign bit (ISOFT2) and two soft decision bits.

QSOFT(2:0) This bus is the Q channel soft decision slicer output data, expressed in 2's complement format with one sign bit (ISOFT2) and two soft decision bits.

IEND(7:1) This bus is the 7 MSB's of I end symbol sample into the soft decision slicer, in 2's complement format. (MSB = Iend7).

QEND(7:1) This bus is the 7 MSB's of Q end symbol sample into the soft decision slicer, in 2's complement format. (MSB = Qend7).

Status Signal Bus

STATUS(6:0) This bus contains 7 bits of demodulator status. These bits are defined as:

STATUS 6 Carrier Tracking Loop Lock: 1 = Locked; 0 = Not Locked.

STATUS 5 Acquisition/Tracking Indicator: 1 = Acquisition Parameters being used by Carrier and Bit Phase Tracking Loops; 0 = Tracking Parameters being used in Carrier and Bit Phase Tracking Loops.

STATUS 4 Not Used.

STATUS 3 Frequency Sweep Direction: 1 = Increasing in Frequency; 0 = Decreasing in Frequency.

STATUS 2 High Power: This bit indicates whether the AGC is at its lower limit. 1 = AGC at lower limit; 0 = AGC above lower limit.

STATUS 1 Low Power: This bit indicates whether the AGC is at its upper limit. 1 = AGC above the upper limit; 0 = AGC at or below the upper limit.

STATUS 0 Data Ready Strobe: This bit pulses high (1) for one clock synchronous with a new signal output on OUTB6-0.

Status Signal Parameter Busses

AGC(7:1) This bus is the 7 MSB's of the AGC Accumulator Register. (MSB = AGC7).

MAG (7:0) This bus is the eight bit magnitude output of the Cartesian to Polar converter, in unsigned binary format. (MSB = MAG7).

PHASE (7:0) This bus is the eight bit phase output of the Cartesian to Polar converter, in unsigned binary format. (MSB = PHASE7).

FE(7:1) This bus is the seven MSB's of the Frequency Error Detector Output Register, in 2's complement format. (MSB = FE7).

GE (7:1) This bus is the seven MSB's of the Gain Error (AGC) Accumulator Register, in 2's complement format. (MSB = GE7).

TE (7:1) This bus is the seven MSB's of the Bit Phase Error Detector Output Register, in 2's complement format. (MSB = TE7).

CARPE (7:1) This bus is the seven MSB's of the Carrier Phase Error Detector Output Register, in 2's complement format. (MSB = PE7).

LKACC(6:0) This bus is the seven MSB's of the Phase Error Accumulator Register in the Lock Detector, in unsigned offset binary format. (MSB = LKACC6).

LKCNT(6:0) This bus is the seven MSB's of the Integration Counter in the Lock Detector, in one's complement format. (MSB = LKCNT6).

NCOCOS(9:0) This bus is the 10 bit two's complement output of the DCL NCO, in 2's complement format. (MSB = NCOCOS7).

Applications for the Various Output Signals

ISOFT(2:0) and QSOFT(2:0) These signals provide a simple interface to a FEC decoder. As the most likely to be used output bus, these signals are included in all but one of the programmable multiplexer output configurations.

IEND(7:1) and QEND(7:1) These signals are useful when input to a D/A converter and displayed on an oscilloscope in the X-Y plot. This will yield the constellation signal display with which analog modem designers are familiar.

STATUS(6:0) These signals can be used in fault detection for use in BIT/BITE Applications and are useful during system debug.

AGC(7:1) This signal is useful in monitoring the AGC operation, signal detection and Antenna Tracking Applications. Other single bit signals are provided for direct use in external AGC.

MAG(7:0) and PHASE(7:0) These signals are useful in signal detection applications, where presence of a signal is represented by a particular signal magnitude or phase.

FREQERR(7:1), GAINERR(7:1), BITPHERR(7:1), and CARPHERR(7:1) These signals are useful in applications that need these signals output at the symbol rate and available for hardwiring, rather than at the processor access rate. Configurations that use the DCL as a stand alone demodulator and matched filter are examples of such applications.

LKACC(6:0) and LKCNT(6:0) These signals are provided for applications which require a lock detection interface that is not processor dependent. These signals are also useful in fault detection in BIT/BITE Applications.

NCOCOS9-0 This signal is provided for use when the DCL is configured as a stand alone Loop Filter and NCO. This signal can be useful in fault detection in BIT/BITE Applications.

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